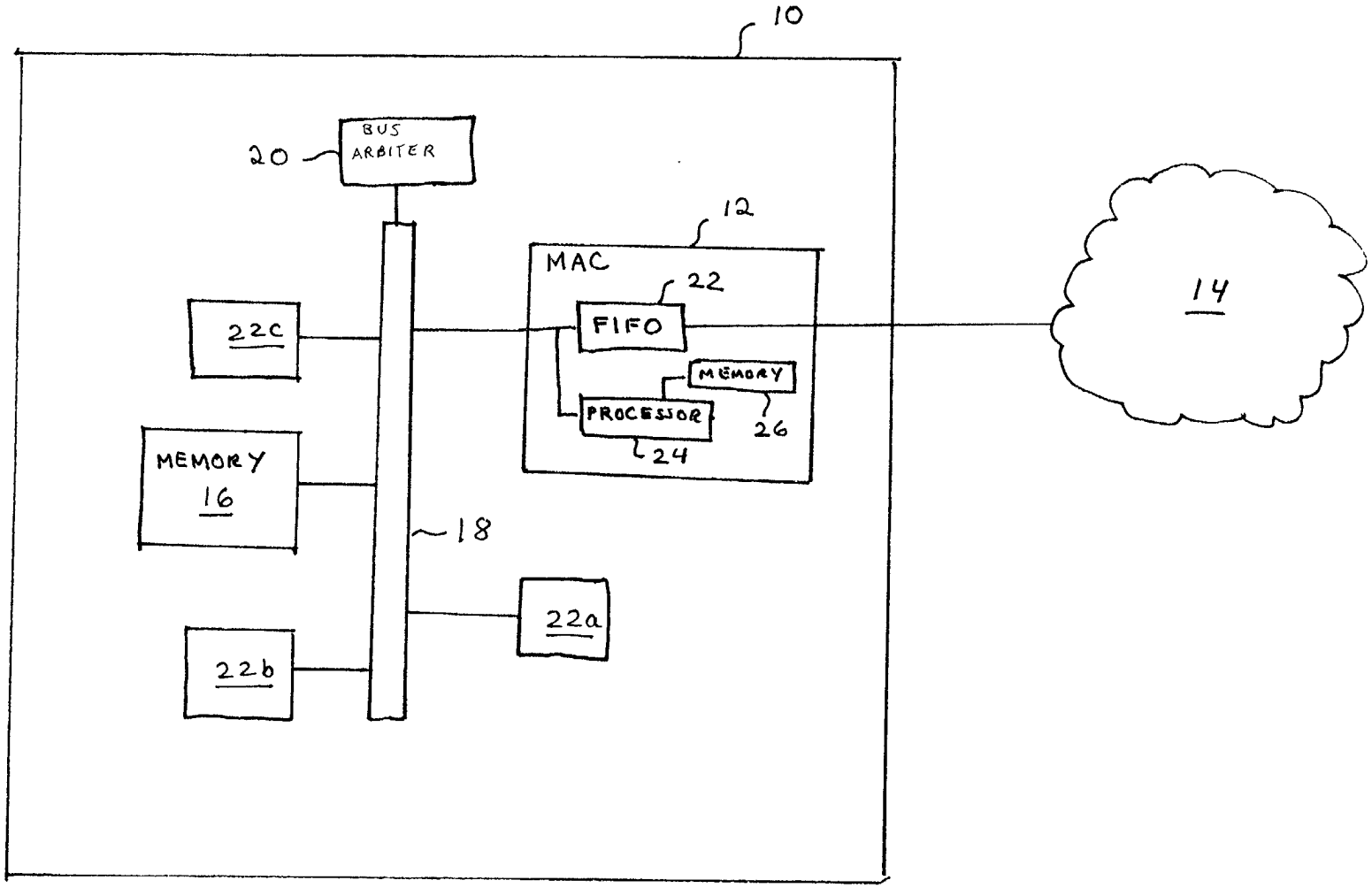
10
20
BUS ARBITER
12
MAC
22
FIFO
MEMORY
26
PROCESSOR
24
14
22c
MEMORY
16
18
22a
22b

FIG. 1

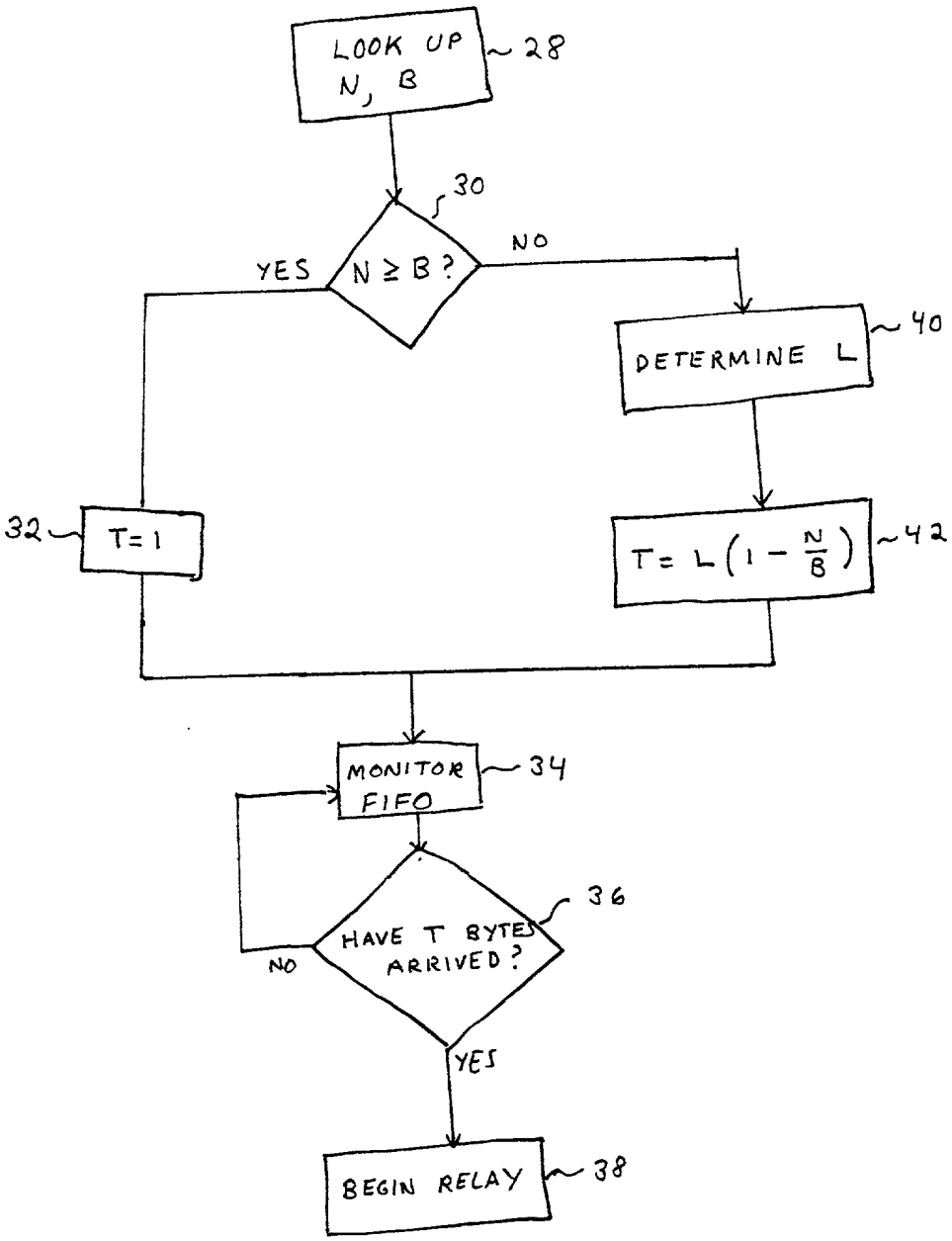
LOOK UP N, B
28
30
N ≥ B ?
YES
NO
DETERMINE L
40
32
T = 1
T = L(1 − N/B)
42
MONITOR FIFO
34
HAVE T BYTES ARRIVED ?
36
NO
YES
BEGIN RELAY
38

FIG. 2

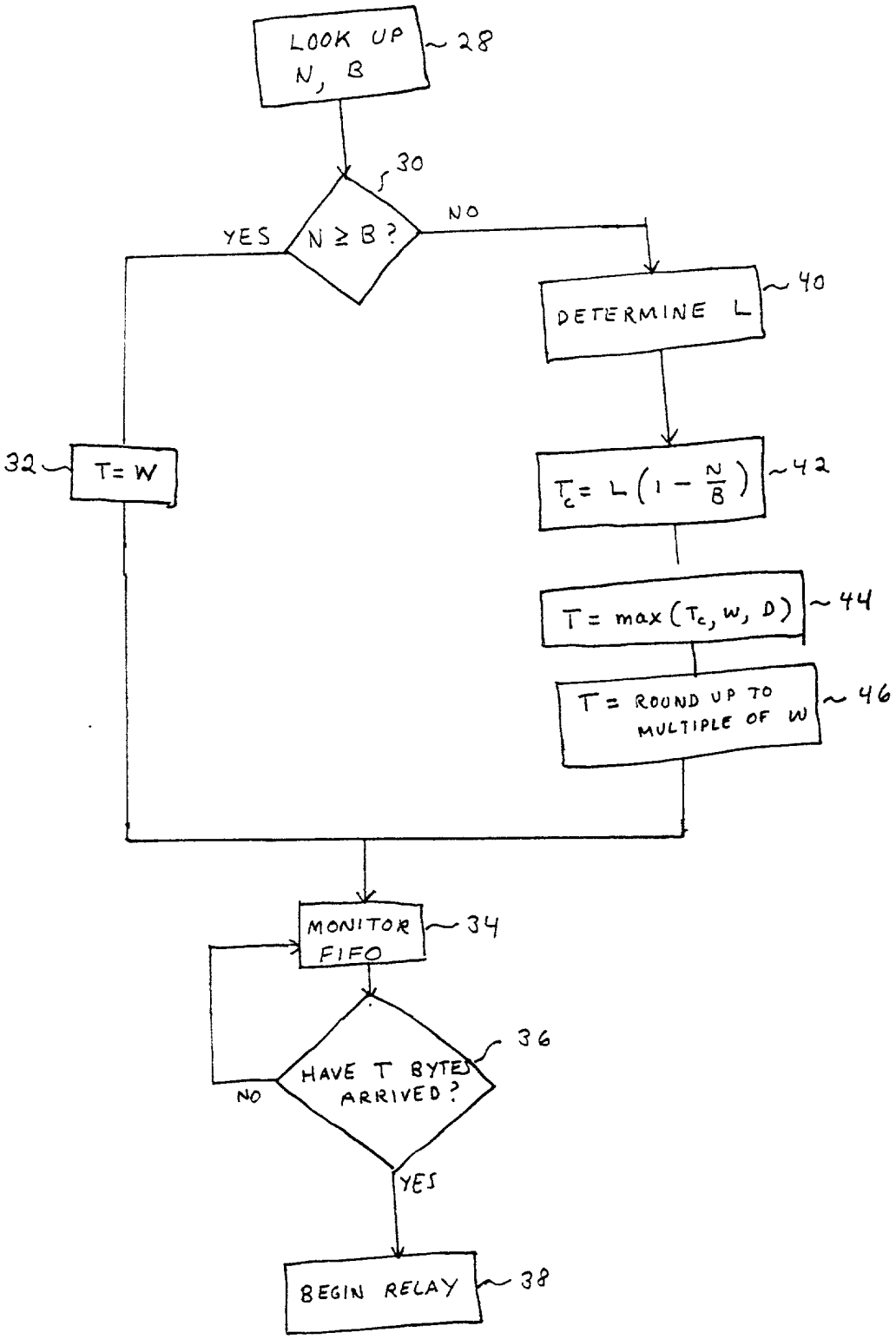
LOOK UP N, B
28
30
N ≥ B ?
YES
NO
32
T = W
DETERMINE L
40
$T_c = L\left(1 - \frac{N}{B}\right)$
42
T = max (T_c, W, D)
44
T = ROUND UP TO MULTIPLE OF W
46
MONITOR FIFO
34
HAVE T BYTES ARRIVED ?
36
NO
YES
BEGIN RELAY
38

FIG. 3

00/22F "STASH/60

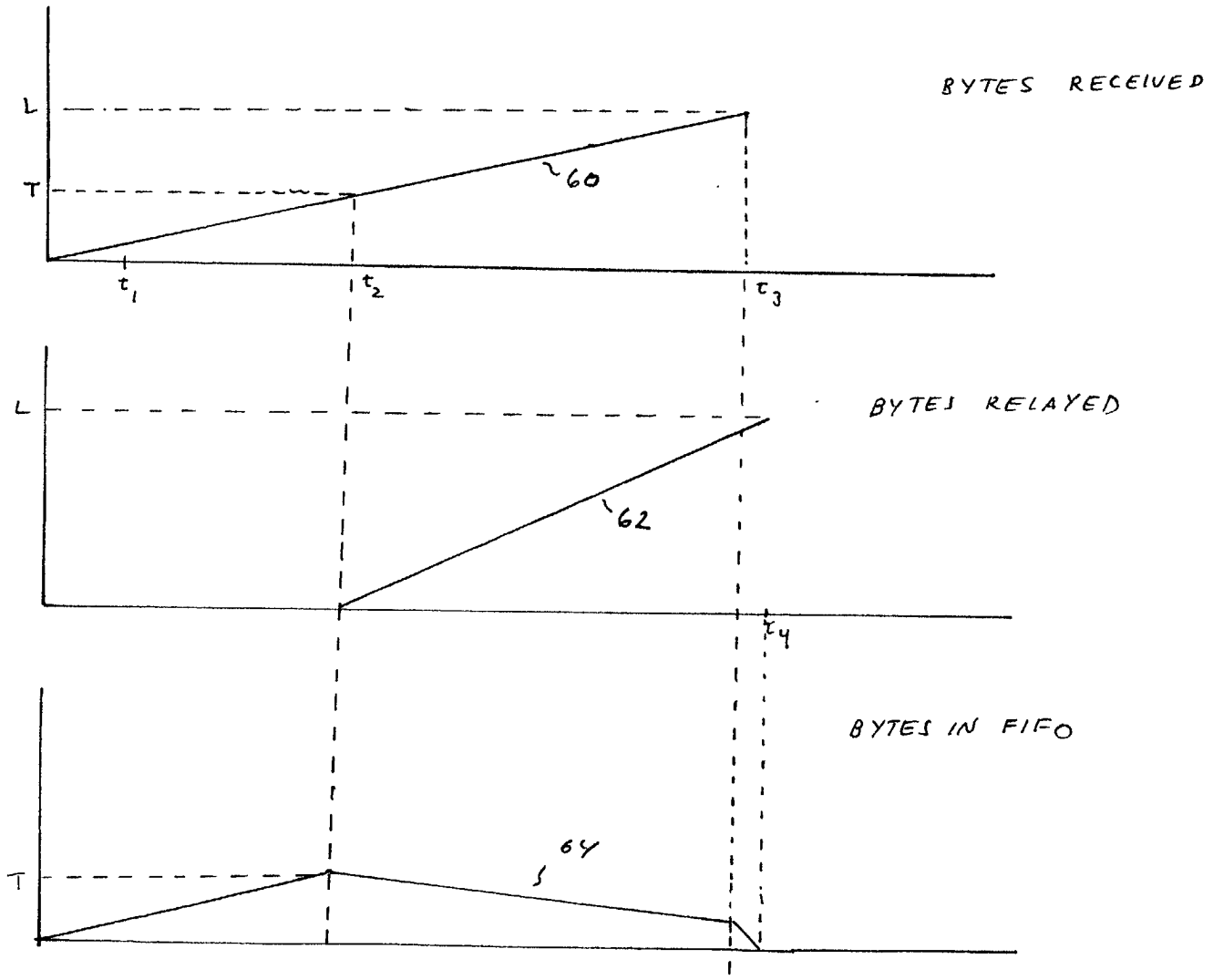

FIG. 4

Normalized Time	Bytes added to FIFO	Bytes transferred	Bytes accumulated in FIFO	Bytes received	Notes
1	1	0	1	0	Start receiving datagram FIFO (at a rate of 1 byte per time unit)
2	1	0	2	0	
3-33	...	0	...	0	Continue receiving datagram
34	1	0	34	0	Controller has now received enough of the header to determine that L=200 bytes
35	1	0	35	0	
36-99	...	0	...	0	
100	1	0	100	0	Enough bytes accumulated in FIFO to begin relay.
101	1	2	99	2	Controller indicates transfer size and begins relay to receiving network.
102	1	2	98	4	Each time unit from here on, 1 byte will be received In the FIFO and 2 bytes will Be written to host memory
103	1	2	97	6	
104-109	...	...	...	...	
150	1	2	50	100	
152-100	...	...	...	...	
200	1	2	2	200	Relay to receiving network is complete

FIG. 5

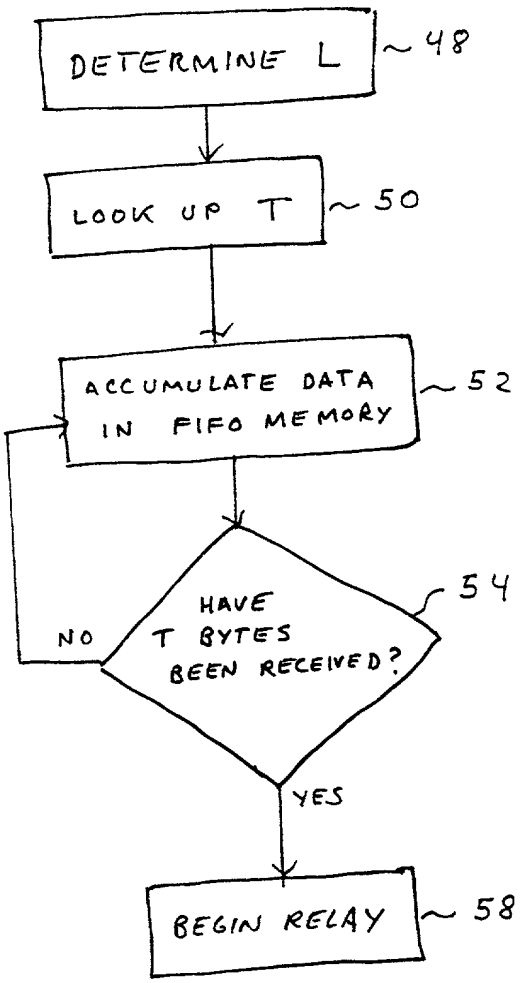
DETERMINE L
48
LOOK UP T
50
ACCUMULATE DATA IN FIFO MEMORY
52
HAVE T BYTES BEEN RECEIVED?
54
NO
YES
BEGIN RELAY
58

FIG. 6